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AMENDMENTS TO THE CLAIMS

1.   (Currently Amended) A ~~Frequency~~ frequency synthesiser according to ~~the~~ a direct digital synthesis method comprising a phase accumulator ~~(1)~~ for ~~the~~ cyclical incrementation of a phase signal ~~(P)~~ by a phase increment ~~(M)~~ present at ~~the~~ an input ~~(3)~~ of the phase accumulator ~~(1)~~, with a memory unit ~~(6)~~ containing a table of sine-function values stored in ~~its~~ memory cells of the memory unit for ~~the~~ determination of sine-function values corresponding to phase values of the phase signal ~~(P)~~, with a digital-to-analogue converter ~~(11)~~ for ~~the~~ conversion of the time-discrete sine-function values into a quasi-analogue sinusoidal time function and with an anti-aliasing low-pass filter ~~(16)~~ for smoothing the quasi-analogue sinusoidal time function, ~~characterised in that~~ wherein

a non-periodic signal ~~(NS)~~ is superimposed over the time-discrete sinusoidal function values in an adder ~~(19)~~, which is connected between the memory unit ~~(6)~~ and the digital-to-analogue converter ~~(11)~~.

2.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 1, ~~characterised in that~~ wherein the non-periodic signal ~~(NS)~~ is a noise signal.

3.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 2, ~~characterised in that~~ wherein the non-periodic signal ~~(NS)~~ is a noise signal low-pass filtered in the low-frequency range.

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4.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to ~~any one~~ ~~of~~ claims 1 ~~to 3,characterised in that~~ wherein the phase accumulator ~~(1)~~, the memory unit ~~(6)~~, the adder ~~(19)~~ and the digital-to-analogue converter ~~(11)~~ are synchronously timed with a common reference frequency ~~(R)~~.

5.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 4, ~~characterised in that~~ wherein the noise signal bandpass-filtered in the low-frequency range is generated by a noise generator ~~(25)~~, which is controlled with a frequency-divided reference clock pulse ~~(RR)~~ obtained from ~~the~~ a common reference clock pulse ~~(R)~~ by ~~the~~ an intermediate connection of a frequency divider ~~(27)~~.

6.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 5, ~~characterised in that~~ wherein the frequency-divided reference clock pulse ~~(RR) provides~~ has a frequency which is reduced ~~many~~ multiple times by comparison with the common reference clock pulse ~~(R)~~.

7.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 6, ~~characterised in that~~ wherein the noise generator ~~(25) comprises~~ includes:

a pseudo-noise generator ~~(29)~~ for generating a noise signal with a clock-pulse frequency which is reduced ~~many~~ multiple times by comparison with the common reference clock pulse ~~(R)~~;

a first non-recursive filter (40) for interpolating the noise signal generated by the pseudo-

noise generator (29) to a noise signal with a clock-pulse frequency which is reduced many

multiple times by comparison with the common reference signal (R);

a differentiator (45) for filtering a direct component and low-frequency components out

of the noise signal generated by the first non-recursive filter; (40)

and

a second non-recursive filter (41) for interpolating the noise signal generated by the

differentiator (45) to a noise signal with a clock-pulse frequency corresponding to the common

reference frequency (R).

8.   (Currently Amended) The Frequency frequency synthesiser according to claim 7,

characterised in thatwherein the frequency of the frequency-divided reference clock pulse (RR)

and the frequency limiting of the noise signal generated by the pseudo-noise generator (29) is are

reduced four times by comparison with the common reference frequency (R), and the frequency

limiting of the noise signal generated by the first non-recursive filter (40) is reduced twice by

comparison with the common reference frequency (R).

9.   (Currently Amended) The Frequency frequency synthesiser according to claim 7

or 8, characterised in thatwherein the pseudo-noise generator (29) consists of includes two

parallel-connected pseudo-noise generators (30, 31), of which the outputs (32, 33) are

interconnected via a combinatorial logic unit (36).

10.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 3, ~~characterised in that~~ wherein the anti-aliasing low-pass filter ~~(16)~~ is followed by an analogue high-pass filter ~~(52)~~ for ~~the~~ suppression of the noise signal bandpass-filtered in the low-frequency range in an output signal of the anti-aliasing low-pass filter ~~(16)~~.

11.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 10, ~~characterised in that~~ wherein ~~the~~ an output ~~(57)~~ of the analogue high-pass filter ~~(52)~~ is supplied to ~~the~~ a first input ~~(59)~~ of a phase-locking loop ~~(56)~~.

12.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 11, ~~characterised in that~~ wherein the phase-locking loop ~~(56) provides~~ includes:

a phase detector ~~(60)~~ for determining ~~the~~ system deviation between an output frequency signal (F_{DDS}) of the frequency synthesiser present at the output ~~(57)~~ of the analogue high-pass filter ~~(52)~~ and a frequency-divided output frequency signal (F_{PLL}) of the phase-locking loop ~~(56)~~;

a control filter ~~(66)~~ for ~~the~~ dynamic evaluation of the system deviation present at the output ~~(63)~~ of the phase detector ~~(60)~~;

a voltage-controlled frequency oscillator ~~(70)~~ for generating an output frequency signal (F_{PLL}) dependent upon an output signal of the control filter ~~(66)~~; and

a mixer ~~(74)~~ and a series-connected low-pass filter ~~(77)~~ for ~~the~~ coarse conversion of the output frequency signal (F_{PLL}) by ~~the~~ a value of a coarse-grid mixed-frequency signal (F_M) present in the mixer ~~(74)~~.

13.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 12, ~~characterised in that~~wherein a frequency divider ~~(78)~~ for frequency division of the output frequency signal ~~(F_{PLL})~~ coarsely converted by the mixer ~~(74)~~ and a switching element ~~(79)~~, across which the frequency divider ~~(78)~~ can be bridged via a direct connection ~~(84)~~, is connected downstream of the mixer ~~(74)~~.

14.   (Currently Amended) The ~~Frequency~~ frequency synthesiser according to claim 12 ~~or 13~~, ~~characterised in that~~wherein the coarse-grid mixed-frequency signal ~~(F_M)~~ supplied to the mixer ~~(74)~~ of the phase-locking loop ~~(56)~~ is generated by a second phase-locking loop or by conversion from the common reference frequency ~~(R)~~.